AMENDMENTS TO THE CLAIMS

1. (Previously presented) A memory system comprising:

a memory controller;

a bi-directional optical link for transmitting data to and from the memory controller;

at least one memory storage device, each at least one memory storage device comprising a memory-side electro-optical converter coupled to the bi-directional optical link;

a controller-side electro-optical converter for converting communications between the memory controller and the bi-directional optical link;

a wave length detector for detecting a wave length of optical signals sent from the controller-side electro-optical converter and supplying the wave length to the memory controller; and

a wave length adjuster for adjusting the wave length of the optical signals based upon the wave length.

2. (Previously presented) The memory system of claim 1, wherein said memory controller and said at least one memory storage device are arranged and configured to exchange data exclusively through said optical link .

3. (Currently Amended) The memory system of claim 1, wherein said memory controller and said at least one memory storage device are arranged and configured to exchange read/write data through said optical link .

Claims 4-8. (Canceled)

9. (Previously presented) The memory system of claim 1, wherein said bi-directional optical link comprises a plurality of multiplexed optical channels.

Claims 10-14. (Canceled)

15. (Currently Amended) The memory system of claim 9, further comprising:

a multiplexer optically connected with said memory controller arranged and configured for multiplexing said optical channels, and

a demultiplexer optically connected with said at least one memory storage device arranged and configured for demultiplexing said multiplexed optical channels.

16. (Previously presented) The memory system of claim 9, further comprising:

a multiplexer optically connected with said at least one memory storage device arranged and configured for multiplexing optical channels and providing multiplexed optical channels to said bi-directional optical link ; and

a demultiplexer optically connected with said memory controller arranged and configured for demultiplexing said multiplexed optical channels.

17. (Previously presented) The memory system of claim 9, further comprising:

a respective optical multiplexer and demultiplexer on each end of said bi-directional optical link.

18. (Previously presented) The memory system of claim 17, wherein said respective optical multiplexer and demultiplexer are arranged and configured to convert signal data that includes at least read/write data.

19. (Previously presented) The memory system of claim 17, wherein said signal data includes command data.

20. (Previously presented) The memory system of claim 17, wherein said signal data includes address data.

21. (Previously presented) The memory system of claim 17, said signal data includes a clock signal.

22. (Previously presented) The memory system of claim 17, wherein said signal data includes control data.

23. (Previously presented) The memory system of claim 17, further comprising:

electrical data paths connected between said memory controller and said at least one memory storage device.

24. (Previously presented) The memory system of claim 1, wherein said at least one memory storage device is located on a memory module.

25. (Previously presented) The memory system of claim 24, further comprising:

an optical coupler disposed at said memory module arranged and configured to connect said memory storage device to said bi-directional optical link .

Claims 26-27. (Canceled)

28. (Currently Amended) The memory system of claim 1, wherein said memory controller is arranged and configured to provide wavelength adjustment information to said wave length adjuster.

Claims 29-32. (Canceled)

33. (Previously presented) The memory system of claim 1 wherein said data includes read/write data which originates on a plurality of electrical paths, said bi-directional optical link comprising a plurality of discrete optical guides respectively associated with said plurality of electrical paths.

34. (Previously presented) The memory system of claim 1 wherein said data includes command data which originates on a plurality of electrical paths, said bi-directional optical link

comprising a plurality of discrete optical guides respectively associated with said plurality of electrical paths.

35. (Previously presented) The memory system of claim 1 wherein said data includes address data which originates on a plurality of electrical paths, said bi-directional optical link comprising a plurality of discrete optical guides respectively associated with said plurality of electrical paths.

36. (Previously presented) The memory system of claim 1 wherein said data includes clock signal data which originates on an electrical path, said bi-directional optical link comprising a discrete optical guide respectively associated with said electrical path.

37. (Canceled)

38. (Previously presented) The memory system of claim 1 wherein said data includes control signal data which originates on an electrical signal path, said bi-directional optical link comprising a discrete optical guide associated with said electrical signal path.

39. (Canceled)

40. (Currently Amended) The memory system of claim 1, further comprising:

a processor, for communicating with said at least one memory storage device, wherein said memory controller, at least one memory storage device, processor, and bi-directional optical link are all integrated on the same die.

Claims 41-100. (Canceled)

101. (Currently Amended) A method of operating a memory system comprising:

receiving an electrical signal output from a memory controller;

converting said electrical signal output from said memory controller to an optical signal for transmission on an optical path;

providing wavelength information to said memory controller with respect to the optical signal on said optical path;

generating wavelength adjustment information based upon the wavelength information;

adjusting the wavelength of said optical path based on wavelength adjustment information received from the memory controller; and

transmitting said optical signal over the optical path directly to a memory module.

102. (Currently Amended) The method of claim 101, further comprising:

said memory controller receiving data from said memory module through said optical path.

103. (Previously presented) The method of claim 102, wherein said data includes at least one of read/write data.

104. (Currently Amended) The method of claim 102, wherein said data includes address data transmitted from said memory controller to said memory module.

105. (Currently Amended) The method of claim 102, wherein said data includes command data transmitted from said memory controller to said memory module.

106. (Original) The method of claim 102, wherein said data includes a clock signal.

107. (Original) The method of claim 102, wherein said data includes control data.

108. (Original) The method of claim 102, wherein said optical path comprises a plurality of multiplexed optical channels, said data being transmitted over said multiplexed optical channels.

Claims 109-110. (Canceled)

111. (Original) The method of claim 108, further comprising:

multiplexing said optical channels, and

demultiplexing said multiplexed optical channels.

112. (Original) The method of claim 108, further comprising:

multiplexing optical channels and providing multiplexed optical channels to said optical path; and

demultiplexing said multiplexed optical channels.

113. (Original) The method of claim 108, further comprising:

an optical multiplexer and demultiplexer located on each side of said optical path.

114. (Canceled)

115. (Previously presented) The method of claim 101, further comprising:

an optical coupler at said memory module, having a connector for connecting with said optical path.

Claims 116-117. (Canceled)

118. (Currently Amended) The method of claim 101, further comprising:

combining a plurality of electrical paths between said memory controller and memory module into a single optical path between said memory controller and memory module.

119. (Currently Amended) The method of claim 118 wherein said single optical path further passes command data between said memory controller and memory module.

120. (Currently Amended) The method of claim 118 further comprising:

passing address data between said memory controller and memory module along said single optical path.

121. (Canceled)

122. (Currently Amended) The method of claim 101, further comprising:

integrating a processor for communicating with said memory module with said memory controller, memory module, and optical path all within the same die.

Claims 123-150. (Canceled)

151. (Original) The memory system of claim 9, wherein said plurality of multiplexed optical channels use Time Division Multiplexing (TDM).

152. (Original) The memory system of claim 9, wherein said plurality of multiplexed optical channels use Wave Division Multiplexing (WDM).

153. (Previously presented) The memory system of claim 9, wherein said plurality of multiplexed optical channels use Frequency Division Multiplexing (FDM).

154. (Original) The memory system of claim 1, wherein said optical path optically passes compressed data.

Claims 155-158. (Canceled)

159. (Original) The method of claim 108, wherein said plurality of multiplexed optical channels use Time Division Multiplexing (TDM).

160. (Original) The method of claim 108, wherein said plurality of multiplexed optical channels use Wave Division Multiplexing (WDM).

161. (Previously presented) The method of claim 108, wherein said plurality of multiplexed optical channels use Frequency Division Multiplexing (FDM).

162. (Original) The method of claim 101, wherein said step of transmitting further comprises transmitting compressed data.

163. (Canceled)